AMC-V6
DATASHEET

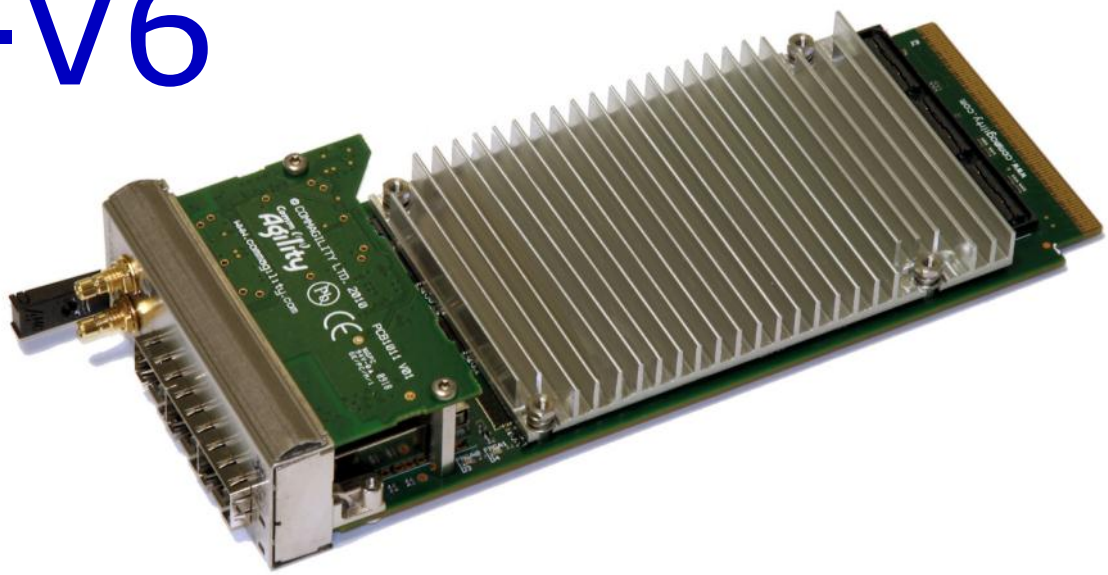
A high performance Virtex-6 FPGA based AMC card with high speed, flexible I/O

Ideal for wireless radio head interface applications requiring multiple 6G CPRI links

FPGA size up to LX550T possible for the most demanding applications

Front panel I/O options of triple SFP+ or dual mini-SAS

Synchronisation via front panel or AMC TCLKs; GPS receiver option



KEY FEATURES

RESULTING BENEFITS

• Xilinx Virtex-6 FPGA	⇒ High performance FPGA family
• LX240T-2 FPGA standard build; LX550T-2 FPGA possible	⇒ Cost effective, high density device; largest FPGA available if required
• Two banks of DDR3 SDRAM, one 16-bit, one 32-bit	⇒ Latest external memory technology with multiple high bandwidth buses
• Flash memory	⇒ Storage available for multiple FPGA configurations and additional software
• IDT CPS-1848 Serial RapidIO Gen 2 switch	⇒ SRIO V2.1 at up to 20Gbps per port
• Separate "glue logic" for board configuration and management	⇒ Allows control, FPGA configuration and FLASH reprogramming over SRIO
• Three front panel SFP+ optical interfaces configurable as CPRI, OBSAI, GigE, SRIO or other standards	⇒ Flexible high-speed optical links, especially suitable for wireless applications
• Optional dual mini-SAS	⇒ Flexible high-speed cabled connectivity
• Timing and synchronisation from GPS (optional), front panel or backplane clock I/O	⇒ No additional timing equipment needed, significantly reducing system complexity; syncs easily to wireless test equipment.
• Mezzanine site for additional I/O	⇒ Allows custom requirements to be met
• Single width PICMG AMC.0 R2.0 Advanced Mezzanine Card	⇒ Works with Industry standard MicroTCA chassis; can also run standalone

The CommAgility AMC-V6 is a high performance FPGA-based interface and processing card in the extremely compact Advanced Mezzanine Card form factor. It is powered by a high-density Xilinx Virtex-6 FPGA, and ideal for LTE wireless front-end applications requiring multiple CPRI links at up to 10x (6.144Gbps) line rate.

SRIO V2.1 at up to 20Gbps per port is supported by an IDT CPS-1848 Serial RapidIO switch. The board provides three front panel SFP+ optical interfaces that provide flexible high-speed links, and are configurable as CPRI, OBSAI, GigE, SRIO or other standards. Alternatively, dual mini-SAS connectors offer up to 40 Gbps of front panel I/O. Timing and synchronisation is achieved via GPS, the front panel or backplane clock I/O, and no additional timing equipment is required which significantly reduces system complexity.

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AMC-V6

HARDWARE SPECIFICATIONS

FPGA: Xilinx Virtex-6™ FPGA:
- LX240T-2 standard build, up to LX550T-2 possible for special builds
- Configuration from FLASH or SRIO
- 256 Mbytes x16 DDR3-1066 SDRAM
- 512 Mbytes x32 DDR3-1066 SDRAM
- 128 Mbytes x16 parallel FLASH
- Two 20Gbps 4x SRIO V2.1 links to switch
- Three Gigabit Ethernet ports to switch
- Front panel GTX options: 3x SFP+ or 4x to mini-SAS, each up to 6.25 Gbps
- 4x GTX to AMC ports 20-17

Glue: Embedded glue logic for:
- Configuration of FPGA over SRIO
- Flash update
- General board control via SPI or SRIO: clocks, GPS, SFPs, MMC, UARTs etc.

Timing: full timing and sync support:
- Optional on-board GPS receiver
- Front panel clock input or output
- AMC Telecom clock A-D support
- Configurable PLL and jitter cleaner based on TI CDCE62005 device

Front panel I/O options:
- Triple SFP+ at up to 6.25 Gbps: CPRI, OBSAI, SRIO, Aurora, GigE etc
- Option for dual 20 Gbps mini-SAS: 4x SRIO and 4x FPGA GTX
- SMB for sync clock I/O
- SMB for GPS antenna if fitted

Form Factor:
- Single-width Advanced Mezzanine Card, AMC.0 Rev 2.0 compliant
- Full-size standard product; mid-size possible if no GPS fitted
- IDT CPS-1848™ switch for AMC.4 compliant 20 Gbps x4 connections to AMC ports 4-7 and 8-11
- Broadcom BCM5389 switch for AMC.2 compliant GigE to AMC Ports 0 and 1
- Hot swap support

Debug: FPGA JTAG and serial port via CommAgility Breakout Board (AMC-BB). Additional FPGA JTAG debug connector on underside of board.

Mezzanine: Additional custom front panel I/O possible via mezzanine site: FPGA, GigE and SRIO connections.

Module Management Controller:
- AMC.0 IPMB_L interface
- FRU EEPROM data
- Power & reset, health monitoring

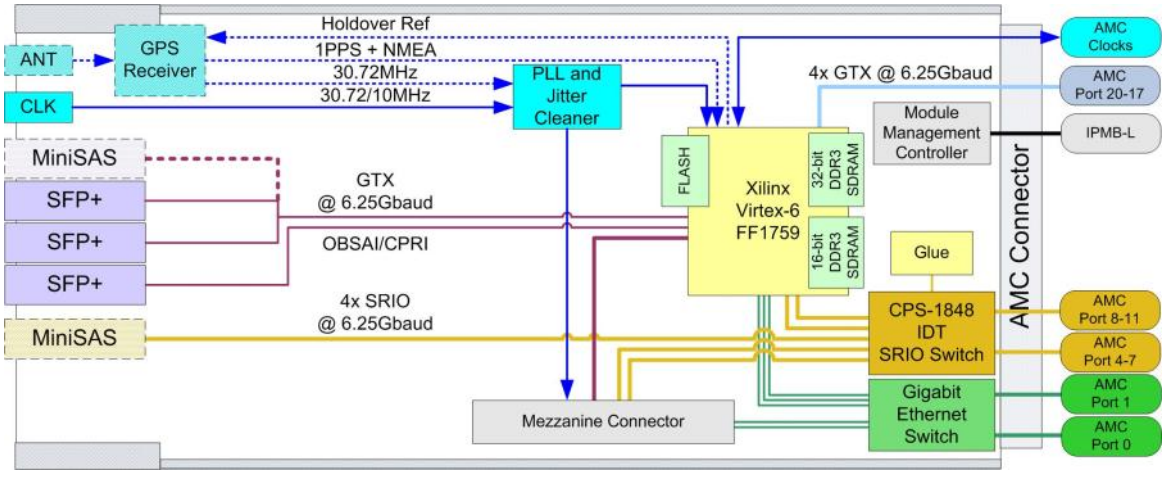
ENVIRONMENT/EMC/SAFETY

- Operating temp: 0-40°C ambient
- Power consumption: up to 30W max
- Designed for NEBS/ETSI compliance when used in appropriate chassis
- 2004/108/EC and FCC EMC compliant
- 2002/95/EC RoHS, 2002/96/EC WEEE and 2006/95/EC LVD compliant

SOFTWARE

Management: Full embedded suite based on Pigeon Point™ Software.

FPGA: Xilinx ISE and EDK project to demonstrate configuration functionality; MicroBlaze BSL including Flash update.



OEM PARTNERSHIP SERVICES:

IN DEVELOPMENT: Support and training; hardware customisation; software and FPGA development.

IN PRODUCTION: lead-time reduction; extended warranty; and repair; quick turn repairs and/or spares stocking.

EXTENDED LIFE: obsolescence management; guaranteed lifecycle; Escrow.

LICENSING is offered for high volume projects.

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